WHAT IS CLAIMED IS:

1. A communication link for use in a data processing system, comprising:

a receive interface to receive and convert the voltage levels of a test signal transmitted over a communication channel, where the test signal carries a clock signal and a test data signal;

a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal; and

a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the communication link, wherein the debug unit further includes a test advisor configured, based on the BER and the at least one jitter characteristic.

2. The communication link of claim 1, further comprising a transmitter including a transmit interface connected to the communication channel and a pattern generator, wherein the transmit interface is connectable to the pattern generator.

3. The communication link of claim 1, wherein the receive interface is configured to convert non-return to zero (NRZ) formatted serial data to parallel CMOS data.

4. The communication link of claim 1, further comprising recommending corrective action responsive to the BER exceeding a specified threshold, wherein the corrective action recommended by the debug unit includes performing at least one additional test when the BER exceeds the predetermined threshold and each of the at least one jitter characteristics is acceptable.

5. The communication link of claim 4, wherein the at least one additional test includes the use of a jitter tolerance pattern.

6. The communication link of claim 1, further comprising recommending corrective action responsive to the BER exceeding a specified threshold, wherein the corrective action recommended by the debug unit includes modifying a characteristic of the CDR when the BER exceeds the predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

7. The communication link of claim 6, wherein said modifying of a characteristic comprises modifying a rate of sampling the transmitted signal by the CDR when the at least one jitter statistic that exceeds the predetermined threshold is a statistic indicative of the high frequency jitter of the communication link.

8. The communication link of claim 6, wherein said modifying of a characteristic comprises modifying a bandwidth of the CDR when the at least one jitter statistic that exceeds the predetermined threshold is a statistic indicative of the communication link's frequency offset.

9. The communication link of claim 1, wherein the CDR circuit includes an edge detector and a phase rotator control unit, wherein an output of the phase detector indicative of the link's high frequency jitter and further an output from the phase rotator control unit indicative of the link's frequency offset are provided to the debug unit.

10. The communication link of claim 1, wherein the debug unit employs and accesses a look up table (LUT) containing a plurality of entries, each entry having an associated BER value and at least one jitter characteristic value, to facilitate the corrective action recommendation.

11. A data processing system, comprising:

a first device connected to a communication channel, the first device including a communication link having a pattern generator and a transmit interface to convert a test pattern generated by the pattern generator to a test data signal for transmission via the communication channel;

a second device connected to the communication channel, the second device including a communication link receiver, comprising:

a receive interface to receive and convert the voltage levels of the test data signal transmitted over a communication channel, where the test data signal carries a clock signal and a test data signal;

a clock/data recovery (CDR) circuit coupled to the receive interface and enabled to extract the clock signal and the test data signal from the received signal; and

a debug unit configured to determine a bit error rate (BER) of the test data signal and further configured to determine at least one jitter characteristic of the link, wherein the debug unit further includes a test advisor configured to recommend, based on the BER and the at least one jitter characteristic, corrective action responsive to the BER exceeding a predetermined threshold.

12. The system of claim 11, wherein the corrective action recommended by the debug unit includes performing at least one additional test when the BER exceeds the predetermined threshold and each of the at least one jitter characteristics is acceptable.

13. The system of claim 11, wherein the corrective action recommended by the debug unit includes modifying a characteristic of the CDR when the BER exceeds the predetermined threshold and at least one of the jitter characteristics exceeds a specified threshold.

14. The system of claim 13, wherein said modifying of a characteristic comprises modifying a rate of sampling the transmitted signal by the CDR when the at least one jitter statistic that exceeds the predetermined threshold is a statistic indicative of the link's high frequency jitter.

15. The system of claim 13, wherein said modifying of a characteristic comprises modifying a bandwidth of the CDR when the at least one jitter statistic that exceeds the predetermined threshold is a statistic indicative of the link's frequency offset.

16. The system of claim 11, wherein the CDR circuit includes an edge detector and a phase rotator control unit, wherein an output of the phase detector indicative of the link's high frequency jitter and further an output from the phase rotator control unit indicative of the link's frequency offset are provided to the debug unit.

17. The system of claim 11, wherein the debug unit employs and accesses a look up table (LUT) containing a plurality of entries, each entry having an associated BER value and at least one jitter characteristic value, to facilitate the corrective action recommendation.

18. An integrated circuit, comprising:

a transceiver including a receive interface suitable for connecting the integrated circuit to a serial communication channel;

a clock/data recovery circuit (CDR) connected to the receive interface and configured to extract a clock signal and a test data signal from a signal received via the communication channel;

a debug unit including means for determining a bit error rate (BER) of the test data signal and means for determining at least one jitter characteristic of the communication link and further including means for using the BER and the at least one jitter characteristic to generate an action recommendation if the BER exceeds a specified threshold.

19. The integrated circuit of claim 18, wherein the debug unit includes means for determining high frequency jitter magnitude and frequency offset of the communication link.

20. The integrated circuit of claim 19, wherein the means for generating an action recommendation includes means for accessing a look up table (LUT) to retrieve the action recommendation based on the BER, the high frequency jitter margin, and the frequency offset.